Analysis and Criterion for Inherent Balance Capability in Modular Multilevel DC-AC-DC Converters

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***Abstract*-Modular multilevel dc-ac-dc converters (MMDAC) have emerged recently for high step-ratio connections in medium voltage distribution systems. Extended phase-shift modulation has been proposed and was found to create the opportunity for inherent balance of SM capacitor voltages. This letter presents fundamental analysis leading to clear criterion for the inherent balance capability in MMDAC. A sufficient and necessary condition, with associated assumptions, to guarantee this capability is established. Using the mathematics of circulant matrices, this condition is simplified to a co-prime criterion which gives rise to practical guidance for the design of an MMDAC. Experiments on down-scaled prototypes and simulations on full-scale examples both provide verification of the analysis and criterion for the inherent balance capability of MMDAC.**

***Index Terms*- Inherent voltage balance, modular multilevel dc-ac-dc converters, circulant matrix, MVDC, LVDC**

I. Introduction

The rapid development of high voltage dc (HVDC) transmission and the promising prospect of low voltage dc (LVDC) distribution, as a means to integrate distributed renewable energy and electric vehicles, together provide an impetus to consider bridging the two with medium voltage dc (MVDC) interconnections [1], [2]. Such MVDC could provide controllable and flexible configurations to address growing power demand in urban areas and optimize operation of the distribution networks of the future within a smart grid [3]–[5].

An MVDC distribution system will need a new power electronic interface to connect the MVDC and LVDC networks [5]–[7]. Modular multilevel dc-ac-dc converters (MMDAC) based on dual-active-bridge (DAB) or *LLC* structure have emerged recently [8]–[11] as promising solutions for this application. On the MVDC side, they utilize sub-module (SM) stacks of the modular multilevel converter (MMC) structure to support the medium voltage stress with high modularity and high reliability. A single transformer is used in the internal ac stage to facilitate high step-ratio conversion, in contrast to other modular DAB and *LLC* converters with multiple transformers and associated insulation challenges [6], [12], [13]. The LVDC side of MMDAC has the structure of classic DAB or *LLC* circuit and therefore retains the benefits of soft-switching operation leading to good efficiency.

Noting that the number of SMs in each stack of MMDAC is much less than that in a classic MMC for HVDC applications [14], an extended phase-shift modulation scheme [8], [15] was developed for MMDAC and was found to feature inherent balance of their SM capacitor voltages for some operating cases. Inherent balance is important for MMDAC because it can reduce the complexity of the complete control algorithm and thus ease the requirements placed on the controller hardware. It obviates the large computational burden of the real-time sorting and rotation needed in conventional MMC modulation schemes [14], which is usually conducted on expensive Field Programmable Gate Arrays (FPGAs), and it also avoids high speed communication between the controller and the SM. Further, the inherent balance capability allows the converter to revert to working in open-loop, with SM voltage balance maintained, if a sensor or feedback loop fails, and this increases the system reliability of MMDAC. Lastly, it can also benefit the hardware design since the switching frequency, voltage stress and current stress are equal for all SMs and tighter SM design limits can be specified, which could reduce the overall cost of the SM switches, SM capacitors and SM heat sink in MMDAC.

However, these benefits of inherent balance in MMDAC are comprised because its existence had only been demonstrated in some particular operating cases of specific MMDAC topologies [8], [11], [15] and was known to be absent in other cases [9], [16]. The mechanism and criterion for inherent balance have not been not fully understood and only empirical rules of thumb were given in [16]. This letter reformulates switching sequence of the phase-shift modulation [8], [15] as a circulant matrix to capture its feature of cyclically linking the state of the last SM in the stack back to the first. Based on this formulation, a sufficient and necessary condition, with associated assumptions, for inherent balance capability in MMDAC is established. Using the mathematics of circulant matrices [17]–[19], this condition is simplified to a co-prime criterion which gives rise to practical guidance for the design of an MMDAC. Based on these new discoveries, the phase-shift modulation is renamed circulant modulation in this letter to highlight its linkage with circulant matrices. A set of experiments and simulations verifies the analysis and criterion for the inherent balance capability.

II. Inherent Balance Capability

The schematic of the DAB-based MMDAC is shown in Fig.1. The MVDC side contains two stacks of half-bridge SMs, and each stack comprises n SMs. Together they form a single-

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phase MMC arrangement with arm inductors L_T and L_B. The connection points for SM stacks and arm inductors are named as A for the top arm and B for the bottom. The primary winding N_1 and magnetizing inductor L_M of the internal transformer ($r_T = N_1/N_2$) is connected between the phase midpoint C and a neutral point D created by two dc link capacitors C_{MT} and C_{MB}. The average voltages on these two capacitors are assumed to be equal at V_M. On the LVDC side, a full-bridge circuit connects the transformer secondary winding N_2 to a smoothing capacitor C_L on the LVDC link. The topology of the *LLC*-based of MMDAC is almost the same but with an extra resonant capacitor C_r between the phase midpoint and transformer primary winding, as shown by the dashed connection in Fig. 1.

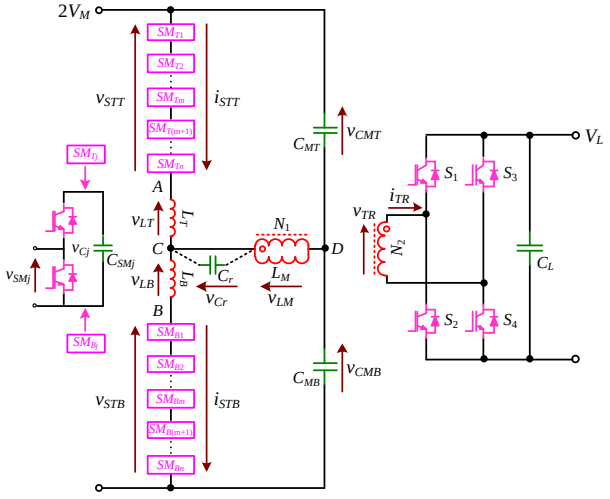

Fig. 1. Schematics of the DAB-based or *LLC*-based of MMDAC.

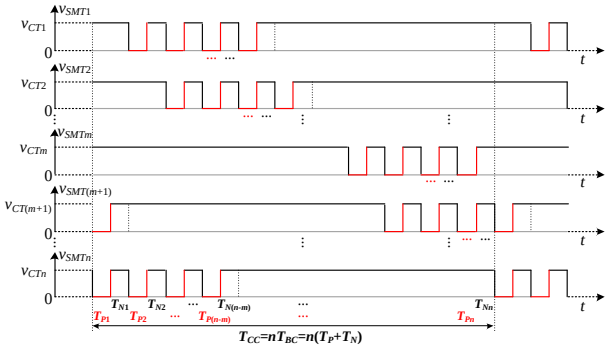

Fig. 2. Circulant modulation scheme for MMDAC (For each SM, red period means its capacitor bypassed, black period means its capacitor inserted).

For the DAB-based MMDAC, the top and bottom stacks generate a pair of complimentary square-wave voltages v_{STT} and v_{STB}, leading to identical low square-wave voltages v_{AD} and v_{BD} across the internal ac-stage passive network. The voltage v_{CD} imposed by the LVDC link V_L and set by the LVDC side full-bridge inverter has a phase shift angle φ with respect to v_{AD} and v_{BD}. The angle φ is used to control the current flow between MVDC and LVDC links as in the classic DAB converter, and the arm inductors L_T and L_B form a parallel connection and play the equivalent role as the phase-shift inductor in classic DAB converter [13]. For the *LLC*-based MMDAC, the top and bottom stacks also need to generate a pair of complimentary square-wave voltages and create identical low square-wave voltages v_{AD} and v_{BD} to excite the resonance between the arm inductor, magnetizing inductor, and resonant capacitor, which constitutes the resonant tank as in the classic *LLC* converter.

By switching either m or n SM capacitors into the circuit ($1 \le m < n$) for equal time durations, a SM stack can readily generate a square-wave voltage. Taking the top stack as the example, the positive stage is defined as m SMs switched in (the remainder, $n-m$, SMs are bypassed) for a period denoted as T_P. In this state, the top stack voltage v_{STT} is smaller than V_M and v_{AD} is positive. The negative stage is defined as all, i.e., n SMs switched in and its time period is set equal to the positive stage ($T_N = T_P$). In this state, the top stack voltage v_{STT} is larger than V_M and v_{AD} is negative. With the circulant modulation [8], [15], the driving signal for each SM has a time shift of $T_P + T_N$ with respect to the previous one and the signal of the last SM is the reference for the first. Each SM capacitor is inserted into and bypassed from the circuit in a preset circular sequence, and the SM output voltages, v_{SMTj} ($j = 1,2,\cdots,n$), forms a sequence of voltage pulses with a circular shift of $T_P + T_N$, shown in Fig. 2.

Considering the voltage loop of the top arm during the first positive stage T_{P1} yields (1), and the equivalent circuit is shown in Fig. 3(a).

$$v_{CMT} - v_{STT} = v_{CMT} - \sum_{j=1}^{n} v_{SMTj} = v_{CMT} - \boldsymbol{S_{P1T}} \cdot \boldsymbol{v_{CT}}^{\boldsymbol{T}} = v_{AD} \quad (1)$$

where v_{CMT}, v_{STT}, and v_{AD} are the instantaneous voltages for top link capacitor, top SM stack and internal ac-stage passive network. For the DAC-based MMDAC, $v_{AD} = v_{LT} + v_{LM}$. For the *LLC*-based MMDAC, $v_{AD} = v_{LT} + v_{Cr} + v_{LM}$. $\boldsymbol{v_{CT}} = [v_{CT1} \quad v_{CT2} \quad \cdots \quad v_{CTn}]$, which is a n dimensional voltage vector for each instantaneous SM capacitor voltage. $\boldsymbol{S_{P1T}} = [\overbrace{1 \quad 1 \quad \cdots \quad 1 \quad 1}^{m} \quad \overbrace{0 \quad 0 \quad \cdots \quad 0 \quad 0}^{n-m}]$, which is a n dimensional switching vector to indicate the on or off (1 or 0) state of each SM in top stack for T_{P1}. In other words, during the first positive stage, m capacitors from SM_{T1} to SM_{Tm} are inserted into the circuit while the remaining $n-m$ capacitors from $SM_{T(m+1)}$ to SM_{Tn} are bypassed.

The relationship in the following negative stage T_{N1} is shown in (2), where $\boldsymbol{S_{N1T}} = [\overbrace{1 \quad 1 \quad \cdots \quad 1 \quad 1}^{n}]$. All n SM capacitors are inserted, and the equivalent circuit is given in Fig. 3(b).

$$v_{CMT} - \boldsymbol{S_{N1T}} \cdot \boldsymbol{v_{CT}}^{\boldsymbol{T}} = v_{AD} \quad (2)$$

The second positive stage, T_{P2}, can still be expressed by (1) but with the switching vector $\boldsymbol{S_{P2T}}$ replacing $\boldsymbol{S_{P1T}}$. The vector $\boldsymbol{S_{P2T}}$ for T_{P2} is generated from $\boldsymbol{S_{P1T}}$ with a circular shift of all the elements such that the state (1 or 0) of SM_{T1} is moved to SM_{T2} and so on plus the state of SM_{Tn} is moved to SM_{T1}, i.e., $\boldsymbol{S_{P2T}} = [\overbrace{0 \quad 1 \quad \cdots \quad 1 \quad 1}^{m} \quad \overbrace{1 \quad 0 \quad \cdots \quad 0 \quad 0}^{n-m}]$. There are still m capacitors inserted in T_{P2} but they are now SM_{T2} to $SM_{T(m+1)}$. The remaining $n-m$ capacitors from $SM_{T(m+2)}$ to SM_{Tn} plus SM_{T1} are bypassed. The following negative stage, T_{N2}, is still described by (2) since all the SM capacitors are inserted again. The equivalent circuits for T_{P2} and T_{N2} are shown in Fig. 3(c) and Fig. 3(d) respectively.

This pattern continues such that the switching vector for nth positive stage, T_{Pn} (the last positive stage), is written as $\boldsymbol{S_{PnT}} =$

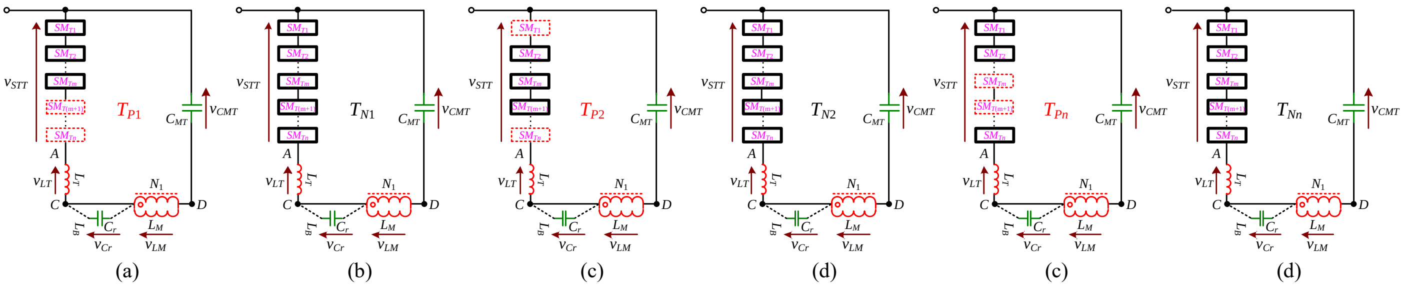

Fig. 3. Equivalent circuits of the voltage loop of the top arm from T_{P1} to T_{Nn} within one circulant cycle. (a) During T_{P1}. (b) During T_{N1}. (c) During T_{P2}. (d) During T_{N2}. (e) During T_{Pn}. (f) During T_{Nn}. (For each SM, red dashed box means its capacitor bypassed, black bold box means its capacitor inserted).

$\Big[\overbrace{1 \quad 1 \quad \cdots \quad 1 \quad 0}^{m} \quad \overbrace{0 \quad 0 \quad \cdots \quad 0 \quad 1}^{n-m}\Big]$ for the voltage relationship in (1). This means m capacitors from SM_{T1} to $SM_{T(m-1)}$ plus SM_{Tn} are inserted into the circuit while the remaining $n-m$ capacitors from SM_{Tm} to $SM_{T(n-1)}$ are bypassed. The corresponding equivalent circuit is given in Fig. 3(e). After the following negative stage T_{Nn}, shown in Fig. 3(f), which is still expressed by (2), the top stack operation returns to T_{P1} and the switching vector goes back to $\boldsymbol{S_{P1T}}$ for the relationship in (1).

A positive stage and the following common negative stage constitute one base cycle, T_{BC}, and $T_{BC} = T_P + T_N$. This is the operation cycle for dc link capacitor and internal ac-stage passive network. A full set of the base cycles taken together constitutes one circulant cycle, T_{CC}, and $T_{CC} = nT_{BC}$. This is the operation cycle for all the SM capacitors. The switching cycle T_{SC} for all the SM switches is equal to $\frac{n}{n-m}T_{BC}$, and this means the SM switching frequency is lower than the internal ac-stage fundamental frequency for all the operation cases.

In steady-state operation, the integral of v_{AD} over a base cycle is 0 for both DAB-based and *LLC*-based MMDAC. Combining (1) and (2) for a base cycle integral yields, the average values of each individual SM capacitor voltage as shown in (3).

$$\boldsymbol{S_{P1T}} \cdot \boldsymbol{\bar{v}_{P1CT}^T} + \boldsymbol{S_{N1T}} \cdot \boldsymbol{\bar{v}_{N1CT}^T} = 2V_M \tag{3}$$

where $\boldsymbol{\bar{v}_{P1CT}} = [\bar{v}_{P1CT1} \quad \bar{v}_{P1CT2} \quad \cdots \quad \bar{v}_{P1CTn}]$ and $\boldsymbol{\bar{v}_{N1CT}} = [\bar{v}_{N1CT1} \quad \bar{v}_{N1CT2} \quad \cdots \quad \bar{v}_{N1CTn}]$, which are voltage vectors for the average value of each instantaneous SM capacitor voltage for T_{P1} and T_{N1}. Noting that the average voltage difference for each SM capacitor between the short positive stage and negative stage is very small and that the difference in average value between base cycles within one circulant cycle is negligible compared to the medium voltage $2V_M$, equation (3) can be written as (4).

$$\begin{aligned}&\boldsymbol{S_{P1T}} \cdot \boldsymbol{\bar{v}_{P1CT}^T} + \boldsymbol{S_{N1T}} \cdot \boldsymbol{\bar{v}_{N1CT}^T}\\ &\approx \boldsymbol{S_{P1T}} \cdot \boldsymbol{\bar{v}_{1CT}^T} + \boldsymbol{S_{N1T}} \cdot \boldsymbol{\bar{v}_{1CT}^T} \approx \boldsymbol{S_{P1T}} \cdot \boldsymbol{\bar{v}_{CT}^T} + \boldsymbol{S_{N1T}} \cdot \boldsymbol{\bar{v}_{CT}^T} = 2V_M\end{aligned} \tag{4}$$

where $\boldsymbol{\bar{v}_{1CT}} = [\bar{v}_{1CT1} \quad \bar{v}_{1CT2} \quad \cdots \quad \bar{v}_{1CTn}]$ and $\boldsymbol{\bar{v}_{CT}} = [\bar{v}_{CT1} \quad \bar{v}_{CT2} \quad \cdots \quad \cdots \quad \bar{v}_{CTn}]$, which are voltage vectors for the average value of each instantaneous SM capacitor voltage for one T_{BC} and T_{CC}.

The circulant cycle T_{CC} is the voltage cycle for all SM capacitors, and so each of $\bar{v}_{CT1}$, $\bar{v}_{CT2}$, $\cdots$, $\bar{v}_{CTn}$ should be a constant (but not necessarily equal) in steady-state operation and their sum is designated as V_{CTS} ($V_{CTS} = \boldsymbol{S_{N1T}} \cdot \boldsymbol{\bar{v}_{CT}^T}$).

Considering all the base cycles in relationship (4), the individual equations can be combined and expressed in (5).

$$\begin{aligned}\boldsymbol{S_{PT}} \cdot \boldsymbol{\bar{v}_{CT}^T} &= \begin{bmatrix}\boldsymbol{S_{P1T}}\\ \boldsymbol{S_{P2T}}\\ \vdots\\ \boldsymbol{S_{PnT}}\end{bmatrix} \cdot \begin{bmatrix}\bar{v}_{CT1}\\ \bar{v}_{CT2}\\ \vdots\\ \bar{v}_{CTn}\end{bmatrix}\\ &= \begin{bmatrix}\overbrace{1 & 1 & \cdots & 1 & 1}^{m} & \overbrace{0 & 0 & \cdots & 0 & 0}^{n-m}\\ 0 & 1 & \cdots & 1 & 1 & 1 & 0 & \cdots & 0 & 0\\ & & \vdots & & & & & \vdots & & \\ 1 & 1 & \cdots & 1 & 0 & 0 & 0 & \cdots & 0 & 1\end{bmatrix} \cdot \begin{bmatrix}\bar{v}_{CT1}\\ \bar{v}_{CT2}\\ \vdots\\ \bar{v}_{CTn}\end{bmatrix} = \begin{bmatrix}2V_M - V_{CTS}\\ 2V_M - V_{CTS}\\ \vdots\\ 2V_M - V_{CTS}\end{bmatrix}\end{aligned} \tag{5}$$

Since $\boldsymbol{S_{PT}}$ is a $n \times n$ matrix, the sufficient and necessary condition for a unique solution of n dimensional vector $\boldsymbol{\bar{v}_{CT}}$ in (5) is that the determinant of $\boldsymbol{S_{PT}}$ is not 0 [17], as written in (6).

$$det(\boldsymbol{S_{PT}}) \neq 0 \tag{6}$$

With this condition established, all the elements in voltage vector $\boldsymbol{\bar{v}_{CT}}$ are linearly independent in (5) which guarantees a unique solution for each of them. Furthermore, analyzing each switching vector, $\boldsymbol{S_{P1T}}, \boldsymbol{S_{P2T}}, \cdots, \boldsymbol{S_{PnT}}$ in matrix $\boldsymbol{S_{PT}}$, it is found that $\boldsymbol{S_{PT}}$ is a circulant matrix [18], which means each element of voltage vector $\boldsymbol{\bar{v}_{CT}}$ plays equivalent role in (5) when $\boldsymbol{\bar{v}_{CT}}$ has a unique solution. Therefore, so long as the voltage vector $\boldsymbol{\bar{v}_{CT}}$ has a unique solution, each element will have an equal value, as shown in (7).

$$\bar{v}_{CT1} = \bar{v}_{CT2} = \cdots = \bar{v}_{CTn} = \frac{2V_M}{m+n} \tag{7}$$

In other words, the sufficient and necessary condition for inherent balance of the average voltages of all SM capacitors in steady-state operation of MMDAC is that the determinant of its switching matrix $\boldsymbol{S_{PT}}$ is not 0. This guarantees that the modulation has a complete rotation for all the SMs within one circulant cycle and therefore energy is fully circulated and shared among all the SM capacitors such that their average voltages are inherently balanced at the value given by (7). In contrast, if $det(\boldsymbol{S_{PT}}) = 0$, there exist linearly dependent elements in $\boldsymbol{\bar{v}_{CT}}$ and its solution is therefore not unique. This implies that the rotation is not complete and there exists redundant and ineffective rotation within one circulant cycle for SMs. Energy is only effectively circulated among subsets of SM capacitors, and so SM capacitor voltages will not be inherently balanced.

It is worth noting that this condition cannot guarantee equal ripple voltage for all the SMs within one circulant cycle because that depends also on individual values of the SM capacitances.

III. Simplified Criterion for Practical Design

The condition in (6) ensures the inherent balance capability in steady-state operation of MMDAC, but the matrix $\boldsymbol{S_{PT}}$ is complex because the SM number in positive stage and negative stage can both be chosen flexibly ($1 \leq m < n$) to create various step-ratios. The determinant of their consequent switching matrix is not straightforward enough to serve as a clear criterion for practical design and operation.

Since $\boldsymbol{S_{PT}}$ is a $n \times n$ circulant matrix, its determinant can be written as (8) using the circulant matrix theory [18], [19].

$$det(\boldsymbol{S_{PT}}) = \prod_{k=0}^{n-1}(1 + 1 \cdot \omega_k + \cdots + 1 \cdot {\omega_k}^{m-1} + 0 \cdot {\omega_k}^{m} + 0 \cdot {\omega_k}^{m+1} + \cdots + 0 \cdot {\omega_k}^{n-1}) \quad (8)$$

where $\omega_k = e^{i2\pi\frac{k}{n}}, k = 0, 1, \cdots, n-1$, which are the nth roots of unity (${\omega_k}^n = 1$) and i is the imaginary unit. Then, the expression (8) is simplified and expressed as (9).

$$det(\boldsymbol{S_{PT}}) = \prod_{k=0}^{n-1}(1 + \omega_k + {\omega_k}^2 + \cdots + {\omega_k}^{m-1}) = \prod_{k=1}^{n-1}\frac{1 - {\omega_k}^m}{1 - \omega_k} \cdot m = \prod_{k=1}^{n-1}\frac{1 - e^{i2\pi\cdot\frac{mk}{n}}}{1 - e^{i2\pi\frac{k}{n}}} \cdot m = \prod_{k=1}^{n-1}\frac{e^{i2\pi} - e^{i2\pi\cdot\frac{mk}{n}}}{e^{i2\pi} - e^{i2\pi\frac{k}{n}}} \cdot m \quad (9)$$

The value of $\frac{mk}{n}$ cannot be an integer if the values of m and n are co-prime (i.e., their only common factor is 1) since k is an integer from 1 to $n-1$ in the last product expression of (9) and thus the value of $det(\boldsymbol{S_{PT}})$ cannot equal 0. If, on the other hand, m and n have a common factor other than 1, i.e., they are not co-prime, there always exists a value of k between 1 and $n-1$ which makes $\frac{mk}{n}$ become an integer and therefore $det(\boldsymbol{S_{PT}})$ will equal 0. It follows that the sufficient and necessary condition (6) for inherent balance capability has been simplified to m and n being co-prime. In other words, so long as the number of SMs switched into positive stage and the number of SMs switched into negative stage are co-prime, the average voltages of all SM capacitor are inherently balanced in steady-state operation. In contrast, if the SM numbers for positive stage and negative stage have a common factor other than 1, the converter will lose this capability. This criterion of m and n being co-prime is much clearer and simper than the matrix condition (6) and provides more practical guidance for designing the circuit and modulation of an MMDAC.

As an example, if $m = 3$ and $n = 4$, the relationships of the average SM capacitor voltages are written in (10).

$$\begin{bmatrix}1 & 1 & 1 & 0\\ 0 & 1 & 1 & 1\\ 1 & 0 & 1 & 1\\ 1 & 1 & 0 & 1\end{bmatrix} \cdot \begin{bmatrix}\bar{v}_{CT1}\\ \bar{v}_{CT2}\\ \bar{v}_{CT3}\\ \bar{v}_{CTn}\end{bmatrix} = \begin{bmatrix}2V_M - V_{CTS}\\ 2V_M - V_{CTS}\\ 2V_M - V_{CTS}\\ 2V_M - V_{CTS}\end{bmatrix} \quad (10)$$

Since m and n are co-prime, the determinant of this switching matrix is not 0. All the average SM capacitor voltages are linearly independent, and they are inherently balanced at the value in (11) derived from (10).

$$\bar{v}_{CT1} = \bar{v}_{CT2} = \bar{v}_{CT3} = \bar{v}_{CT4} = \frac{2}{7}V_M \quad (11)$$

As a contrasting example, with $m = 2$ and $n = 4$, the voltage relationships are given in (12).

$$\begin{bmatrix}1 & 1 & 0 & 0\\ 0 & 1 & 1 & 0\\ 0 & 0 & 1 & 1\\ 1 & 0 & 0 & 1\end{bmatrix} \cdot \begin{bmatrix}\bar{v}_{CT1}\\ \bar{v}_{CT2}\\ \bar{v}_{CT3}\\ \bar{v}_{CTn}\end{bmatrix} = \begin{bmatrix}2V_M - V_{CTS}\\ 2V_M - V_{CTS}\\ 2V_M - V_{CTS}\\ 2V_M - V_{CTS}\end{bmatrix} \quad (12)$$

Because m and n have the common factor of 2, the determinant of this switching matrix is 0 and linearly dependent elements exist. The solution obtained from (12) is not unique for $\bar{v}_{CT1}$, $\bar{v}_{CT2}$, $\bar{v}_{CT3}$, $\bar{v}_{CT4}$, as shown in (13), where K can be an arbitrary constant between 0 and $\frac{2}{3}V_M$ and the solution that will exist in practice depends on the initial state of the circuit. Although there might exist a very specific initial state for the circuit that leads to $K = \frac{1}{3}V_M$ and $\bar{v}_{CT1} = \bar{v}_{CT2} = \bar{v}_{CT3} = \bar{v}_{CT4} = \frac{1}{3}V_M$, the converter in this operating case still needs to be seen as lacking inherent balance capability because it cannot rely, in general, on that specific initial state for the voltage balance of SM capacitors existing.

$$\begin{cases}\bar{v}_{CT1} = \bar{v}_{CT3} = K\\ \bar{v}_{CT2} = \bar{v}_{CT4} = \dfrac{2}{3}V_M - K\end{cases} \quad (13)$$

IV. Down-scaled Experimental Verification

To validate the theoretical analysis, a down-scaled prototype of a DAB-based MMDAC was built first with the parameters listed in Table I. The ac-stage frequency is set at 3 kHz in this down-scaled prototype with consideration of the practical applications of MMDAC for high-power medium-voltage conversion [9], [20]. The SM capacitances have 10% variation from the nominal value due to the manufacturing tolerances.

TABLE I.
DOWN-SCALED EXPERIMENTAL PARAMETERS

Parameter	Description	Value
P	Power Range	0–±500 W
$2V_M$	Medium-side Terminal Voltage	700 V
V_L	Minimum Low-side Terminal Voltage	20 V
C_{SMT} C_{SMB}	DC Link Capacitance	550 µF
L_T L_B	Arm Inductance	7.47 mH
L_m	Magnetizing Inductance	460 mH
r_T	Transformer Turns-ratio	55:22
f_{BC}	Base Frequency, AC-stage Frequency	3 kHz
n	SM Number per stack	4
C_{SMj}	SM Capacitance	50 µF with 10% variation
S	Power Switches	FF225R12ME4

Experimental results for operation with $m = 3$ and $n = 4$ are recorded in Fig. 4. The SM output voltages in Fig. 4(a) show that one SM is bypassed in each positive stage and each SM is bypassed for one positive stage in each circulant cycle. The SMs are inserted into and bypassed from the circuit in a preset circular sequence and the switching frequency f_{SC} of all SMs is equal to a quarter of the base frequency f_{BC} for internal ac stage. This circular shift switching sequence generates the top stack voltage in Fig. 4(b), and the complimentary voltage from bottom stack as also presented. The transformer voltage v_{TRS}, shown in Fig. 4(c), is set an angle φ against the stack voltages to control the current as in the classic DAB. Because m and n are co-prime in this case, the average SM capacitor voltages should be inherently balanced. Here, they are within 2% of 100 V in Fig. 4(d), which is the value predicted from the theoretical analysis in (11). It is worth noting that the low-side terminal voltage and the angle φ can both be freely varied to adjust the power as in the classic DAB circuit and they are not constrained by the modulation pattern providing inherent balance.

Experimental results for operation with $m = 2$ and $n = 4$ are shown in Fig. 5. It can be seen in Fig. 5(a) that two SMs are bypassed in each positive stage and each SM is bypassed for two positive stages in each circulant cycle. The generated stack voltages in Fig. 5(b) still work at angle φ with respect to the

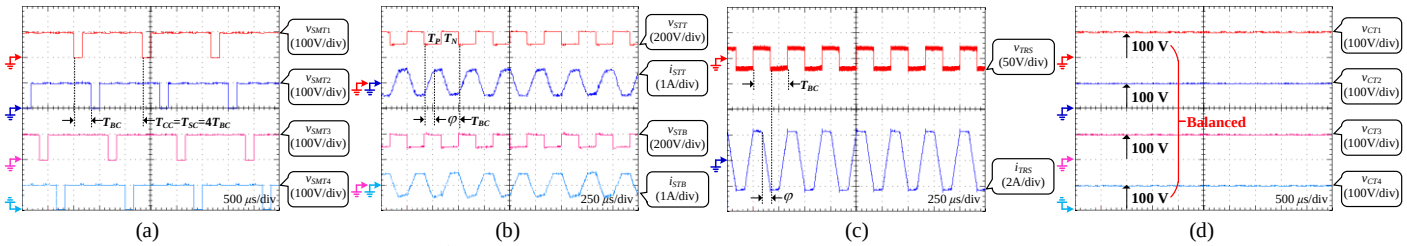

Fig. 4. Experimental results with $m = 3$ and $n = 4$ for DAB-based MMDAC. (a) SM output voltages in top stack. (b) Voltages and currents of top stack and bottom stack. (c) Secondary side transformer voltage and current. (d) SM capacitor voltages of top stack.

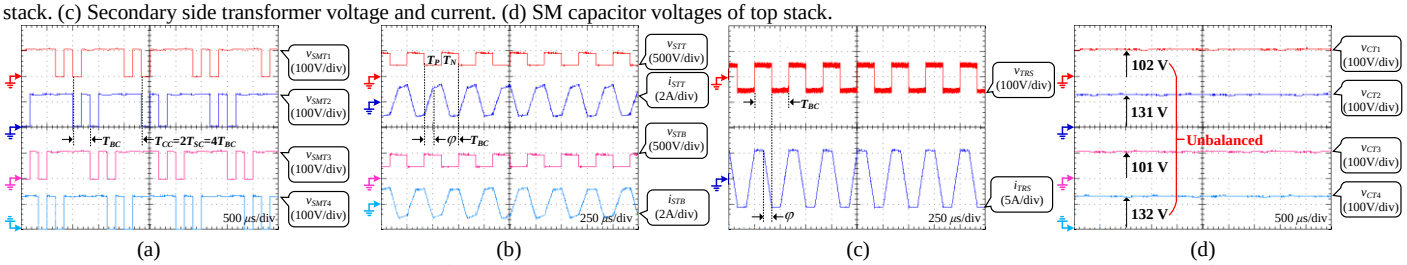

Fig. 5. Experimental results with $m = 2$ and $n = 4$ for DAB-based MMDAC. (a) SM output voltages in top stack. (b) Voltages and currents of top stack and bottom stack. (c) Secondary side transformer voltage and current. (d) SM capacitor voltages of top stack.

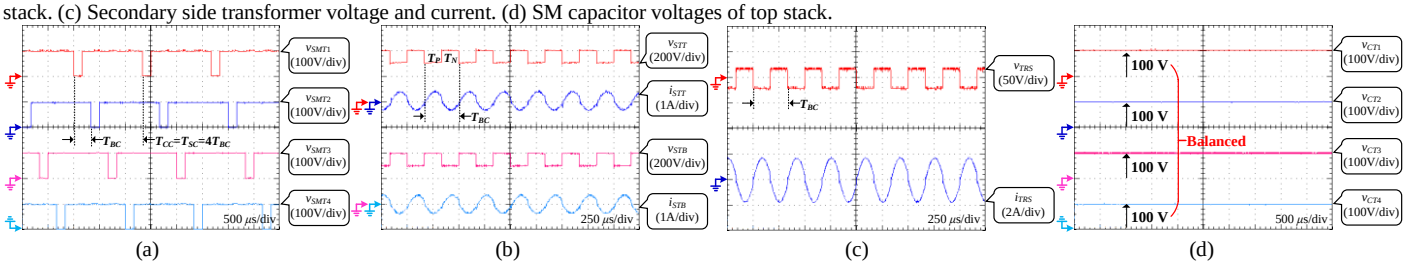

Fig. 6. Experimental results with $m = 3$ and $n = 4$ for *LLC*-based MMDAC. (a) SM output voltages in top stack. (b) Voltages and currents of top stack and bottom stack. (c) Secondary side transformer voltage and current. (d) SM capacitor voltages of top stack.

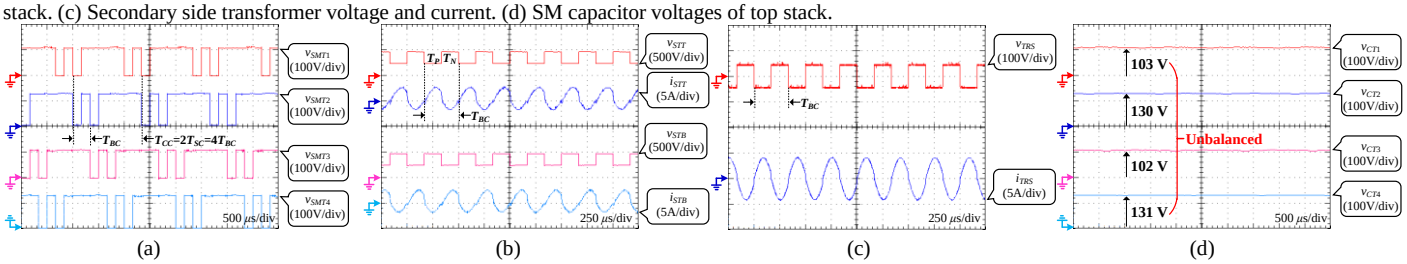

Fig. 7. Experimental results with $m = 2$ and $n = 4$ for *LLC*-based MMDAC. (a) SM output voltages in top stack. (b) Voltages and currents of top stack and bottom stack. (c) Secondary side transformer voltage and current. (d) SM capacitor voltages of top stack.

transformer voltage in Fig. 5(c) to control the current flow. However, the existence of common factor of 2 for m and n in this case removes the inherent balance capability between all SM capacitor voltages. The average SM capacitor voltages shown in the Fig. 5(d) validate the theoretical analysis in (13) and the voltage difference observed between SM capacitors is around 30% of their individual average voltage.

The prototype of DAB-based MMDAC can be readily modified to become an *LLC*-based MMDAC. All circuit parameters remain the same as in Table I but a resonant capacitor ($C_r = 0.824\ uF$) is inserted between the phase midpoint and transformer primary winding, as the connection in Fig. 1.

Experimental results for operation with $m = 3$ and $n = 4$ are shown in Fig. 6. The switching sequence and switching frequency, shown in Fig. 6(a), are the same with those in Fig. 4(a) for DAB-based MMDAC. The generated stack voltage in Fig. 6(b) excites the resonance between arm inductor and resonant capacitor, and the resonant current goes through transformer, shown in Fig. 6(c), before the rectification back to dc. Because m and n are co-prime, all the average SM capacitor voltages have been inherently balanced at 100 V in Fig. 6(d), which further validates the theoretical analysis in (11). The base frequency for internal ac stage can be freely adjusted around the resonant frequency to control the voltage as in the classic *LLC* circuit and it is not constrained by the inherent balance condition. In this case, the base frequency was 3 kHz and the resonant frequency was 2.87 kHz.

Experimental results for operation with $m = 2$ and $n = 4$ are recorded in Fig. 7. The switching sequence and switching frequency in Fig. 7(a) are also the same with those in Fig. 5(a). The generated stack voltage in Fig. 7(b) still excites the resonant operation, and the resonant current trough transformer in this operation case is shown in Fig. 7(c). Because m and n are not co-prime, this *LLC*-based MMDAC also loses the inherent voltage balance capability as expected, shown in Fig. 7(d).

V. Full-scale Simulation Verification

To verify that the analysis and the balance criterion remain

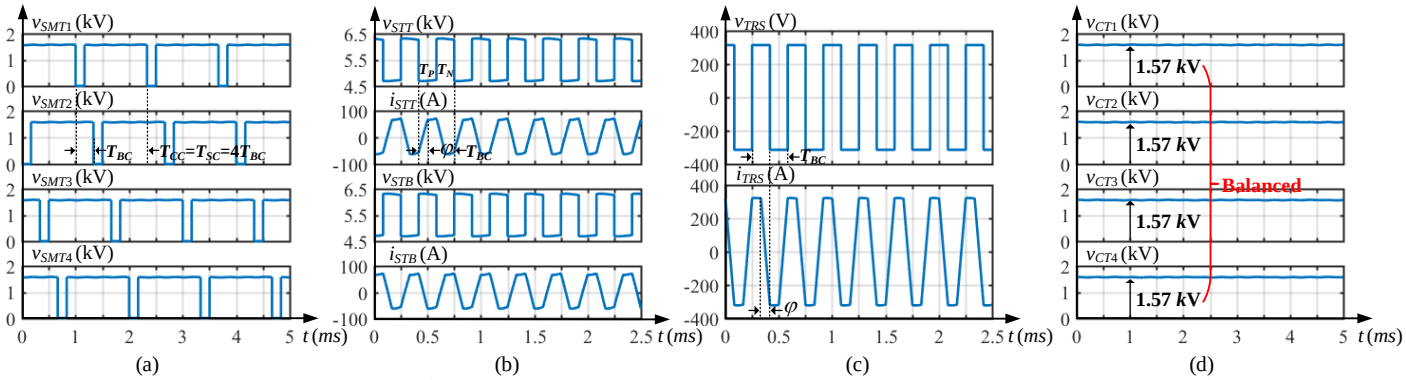

Fig. 8. Simulation results with $m = 3$ and $n = 4$ for DAB-based MMDAC. (a) SM output voltages in top stack. (b) Voltages and currents of top stack and bottom stack. (c) Secondary side transformer voltage and current. (d) SM capacitor voltages of top stack.

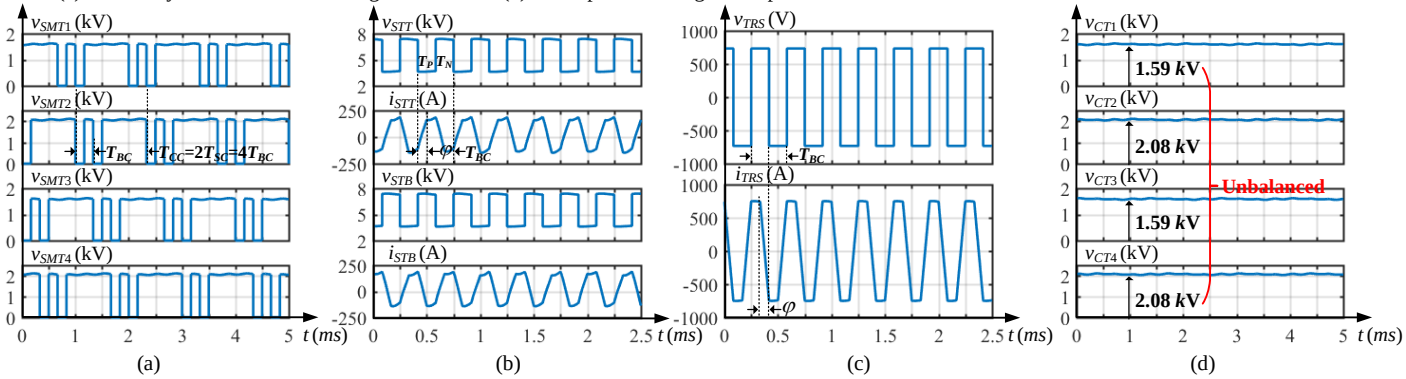

Fig. 9. Simulation results with $m = 2$ and $n = 4$ for DAB-based MMDAC. (a) SM output voltages in top stack. (b) Voltages and currents of top stack and bottom stack. (c) Secondary side transformer voltage and current. (d) SM capacitor voltages of top stack.

valid beyond the down-scaled prototype, a simulation model of DAB-based MMDAC was built for a full-scale medium voltage dc application with the parameters shown in Table II. The SM capacitances were set with 10% variation to reflect manufacturing tolerances.

TABLE II.
FULL-SCALED SIMULATION PARAMETERS

Parameter	Description	Value
P	Power Range	0–±300 kW
$2V_M$	Medium-side Terminal Voltage	11 kV
V_L	Minimum Low-side Terminal Voltage	310 V
C_{SMT} C_{SMB}	DC Link Capacitance	550 µF
L_T L_B	Arm Inductance	0.98 mH
L_m	Magnetizing Inductance	460 mH
r_T	Transformer Turns-ratio	5:2
f_{BC}	Base Frequency, AC-stage Frequency	3 kHz
n	SM Number per stack	4
C_{SMj}	SM Capacitance	500 µF with 10% variation
S	Power Switches	FF450R33T3E3

Simulation results for $m = 3$ and $n = 4$ are presented in Fig. 8. The switching sequence for each SM, shown in Fig. 8(a), is identical to that in Fig. 4(a). The generated stack voltages in Fig. 8(b) work with the transformer voltage in Fig. 8(c) and their phase-shift angle φ can be also utilized to control the power flow between MVDC side and LVDC side. Since m and n are co-prime, the average SM capacitor voltages are inherently balanced at 1.57 kV in Fig. 8(d), which also reaches good agreement with the results in (11).

Simulation results for the contrasting example with $m = 2$ and $n = 4$ are given in Fig. 9. The switching sequence in Fig. 9(a) is identical to that in Fig. 5(a), and the stack voltages in Fig. 9(b) still work with the transformer voltage in Fig. 9(c). Due to the existence of common factor for m and n in this case, the SM capacitor voltages cannot be inherently balanced at one common value, which verifies the results in (13) again.

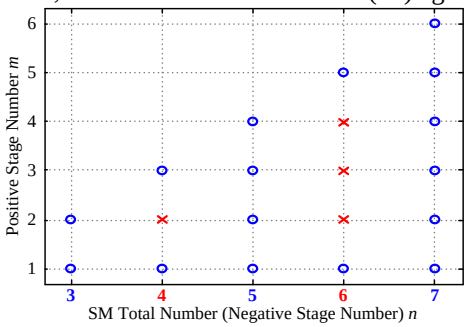

Fig. 10. Inherent balance results in various operation cases.

To further verify the criterion for inherent voltage balance, results for cases with the total number of SM, n, varying from 3 to 7 are summarized in Fig. 10. It can be seen that the SM capacitor voltages are inherently balanced when the total SM number (the negative stage number) n is set at 3, 5 and 7. All of these are prime numbers and cannot have a common factor other than 1 with any positive stage number m ($1 \le m < n$). For $n = 4$ and $n = 6$, the inherent balance capability is lost when m and n are not co-prime ($m = 2, n = 4; m = 2, n = 6; m = 3, n = 6; m = 4, n = 6$). With this in mind, it is recommended that the

total number of SMs in each stack of an MMDAC is chosen to be prime thereby guaranteeing that inherent balance capability is present for all the operation cases.

The full-scale simulation results for the *LLC*-based MMDAC were also conducted by adding a resonant capacitor ($C_r = 6.25\ uF$) to the model of the DAB-based MMDAC. The results are very similar to Fig. 8 to Fig. 10, which also verify the theoretical analysis and criterion. The detailed waveforms are not repeated here to keep the letter concise.

VI. Conclusion

This letter has presented fundamental analysis leading to clear criterion for the inherent balance capability of SM capacitor voltages in modular multilevel dc-ac-dc converters (MMDAC). A sufficient and necessary condition, with associated assumptions, to guarantee this capability in steady-state operation was established. Using the mathematics of circulant matrices, this condition was equivalently simplified to a co-prime criterion which gives rise to practical guidance for the design of an MMDAC. It is recommended that a prime number is chosen for the total SM number in each stack because this guarantees that the inherent balance capability is present in all the operation cases. The experimental results on down-scaled prototypes and simulation results on full-scale examples both verified the theoretical analysis and criterion for MMDAC.

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